INFO: [VRFC 10-163] Analyzing VHDL file "C:/Users/eacm3/Desktop/project\_3/project\_3.srcs/sources\_1/imports/Lab1 prep. work/full adder/full\_adder.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity full\_adder

INFO: [VRFC 10-163] Analyzing VHDL file "C:/Users/eacm3/Desktop/project\_3/project\_3.srcs/sources\_1/imports/Lab1 prep. work/half adder/half\_adder.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity HALF\_ADDER

INFO: [VRFC 10-163] Analyzing VHDL file "C:/Users/eacm3/Desktop/project\_3/project\_3.srcs/sources\_1/imports/Lab1 prep. work/two-input or/twoInputOR.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity OR\_GATE

INFO: [VRFC 10-163] Analyzing VHDL file "C:/Users/eacm3/Desktop/project\_3/project\_3.srcs/sim\_1/imports/full adder/full\_adder\_tb.vhd" into library xil\_defaultlib

INFO: [VRFC 10-307] analyzing entity Testbench\_full\_adder